UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/672,367	09/28/2000	Francis X. McKeen	042390.P9578	7649

7590 11/15/2006	EXAMINER
Blakely Sokoloff Taylor & Zafman	HO, THOMAS M

Blakely Sokoloff Taylor & Zafman
12400 Wilshire Blvd
7th Floor
Los Angeles, CA 90025-1026

ART UNIT	PAPER NUMBER
2132	

DATE MAILED: 11/15/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

	Application No.	Applicant(s)
Office Action Summary	09/672,367	MCKEEN ET AL.
	Examiner	Art Unit	
	Thomas M. Ho	2132	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE _3_ MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
  Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on _24 August 2006_.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) _1-22_ is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) _1-22_ is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All b)☐ Some * c)☐ None of:

      1.☐ Certified copies of the priority documents have been received.

      2.☐ Certified copies of the priority documents have been received in Application No. _____.

      3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☐ Notice of References Cited (PTO-892)

2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3)☐ Information Disclosure Statement(s) (PTO/SB/08)
    Paper No(s)/Mail Date _____.

4)☐ Interview Summary (PTO-413)
    Paper No(s)/Mail Date. _____.

5)☐ Notice of Informal Patent Application

6)☐ Other: _____.

DETAILED ACTION

1.   *The amendment of 8/24/06 has been received and entered.*

Response to Amendments

2.   The Examiner has withdrawn the rejections under 35 USC 101 and 35 USC 112 in light

of Applicant's amendments to the independent claims.

Response to Arguments

3.

The Applicant has argued:

England discloses a software structure for protecting premium content in a nonsecure computer

environment (Abstract and Figure 4) The disclosed computer environment does not provide any

hardware support for protecting memory contents. Instead of using hardware, the teaching of

England relies entirely on software modules for content protection. (Page 6, paragraph 4)

The Examiner contends that England does indeed disclose a general concept of hardware support

.for processor modes and content protection.

The Examiner disagrees with the Applicant's contention that there is no hardware involved in the

mode transition simply because the processor is tied directly to code. For software to properly

function, for any code to properly execute, it is understood that a hardware platform must be

necessary for the software to execute on. If the processor mode transition is dependant on the

code, it follows at a bare minimum, that the processor mode transition is also dependent or

rather, derives support, on the hardware that executes that code. For this reason, the Examiner

disagrees with the assertion that "the teaching of England totally lacks hardware support for the

isolated execution mode."

The Examiner further disagrees with Applicant's assertion because it is clear England et al.

implements the isolated execution mode by using a series of memory rings or circles to support

different modes of execution depending on the location of the executing mode within memory.

More particularly, England employs the usage of an Access control table. (Column 6, line 33 –

Column 7, line 5) to direct the processor on the read write access by storing within the table the

rights of the programs executing in the memory. This memory is directly coupled to the

processor, and the processor receives instructions on how the data is to be accessed and

processed (executed) from the table. (Column 6, line 45-50)

The Applicant has argued: In a paragraph describing processor mode transitions, England

disclose that the mode of a processor is tied directly to the code that is executing (col. 10, lines

13-16). Thus, the mode changes automatically (Col 10. line 17) There is no hardware involved a processor enters a user mode or a secure kernel mode.

Applicant has also argued: (paragraph 7, page 4)

Moreover, with respect to claim 3, the Examiner characterizes the memory manager of England as the claimed memory control hub (MCH). However, the memory manager is not a hardware device coupled between the system memory, the processor, and the graphics card. Rather the memory manager is a software module stored in the system memory. Thus, the physical location and the structure of the memory manager are totally different from the claimed MCH.

The Examiner contends that the memory control hub is both a hardware and software combination that directs the actions of the processors with regards to executing in specific execution modes. (Column 6, lines 33 – Column 7, line 5) The specific execution modes then in turn determine the permittivity of the graphics card to the isolated output area.

Applicant has also argued: (paragraph 7, page 5)

With respect to claim 17, England does not teach or suggest "occluding all windows but the first window." Applicants have carefully reviewed the cited passage and the disclosure in general but have been unable to identify any part of the disclosure that mentions occluding windows"

Applicant's argument has been considered but is moot in view of the new grounds of rejection.

Applicant's further arguments on page 8, paragraph 1 have recited that Cunnif is relied upon for

disclosing image occlusion but does not teach or suggest providing hardware support for the

isolated execution mode of claim 12. This point has been addressed by the new rejection in light

of the amendments made to claim 12 presented below.

Furthermore, Applicant has also argued on page 8, paragraph 1, that Cuniff is disclosed within

the context of a computer graphics display and not with regards to an isolated execution mode.

The Examiner finds this argument to be unpersuasive as it is clear from Applicant's claim 3 that

access to the graphics card and graphics display buffers are dependant upon the platform of

claim 2 being in an isolated execution mode. Applicant's own claim 3 provides an example of

how the nexus between the alleged unrelated fields are in fact, related.

Claim Rejections - 35 USC § 102

4.   The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the

basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5.   Claims 1, 6, 12, 13, 15, 16, 19-22 rejected under 35 U.S.C. 102(e) as being anticipated by

England et al., US patent 6775779.

In reference to claim 1:

England et al. discloses a platform comprising:

- A processor executing in one of a normal execution mode and an isolated execution

    mode, where the processor can execute in different modes and the isolated execution

    mode is the secure mode of execution. (Column 5, lines 35-55)

    o The processor including an isolated execution circuit to provide hardware support

        for the isolated execution mode, where the hardware support for the isolated

        execution mode is provided in the Access control table of (Figure 3), further

        described in (Column 6, lines 45-50) & (Column 6, line 65 – Column 7, line 5)

        The access control table is a hardware circuit, in particular a memory(Column 6,

        lines 33-35) whose information causes the gates to pass or block processor

        read/write controls.

- A system memory accessible to the processor(Column 5, lines 5-35) & (Figure 1, Item

    140, 141) including an isolated area, an isolated output area, and a non-isolated area,

    where the system memory is divided into rings of isolation or protection, and these

    memory areas are one of the means by which the processor executes in isolated execution

    mode. (Figure 2) & (Column 5, line 55 – Column 6, line 12)

- An output device coupled to the processor, where the output device is an I/O adaptor that

    may be a monitor, video card frame buffer or sound card, and where the output device is

    coupled to the processor in that the output devices receive processed information from

the processor. (Figure 1, Item 170, 172) & (Column 4, line 40-55) & (Column 13, lines 1-

50)

In reference to claim 6:

England et al. discloses the platform of claim 1 further comprising:

- An operating system (O/S) nub having a driver to write display data into the isolated

    output area when the processor is executing in the isolated execution mode, where the

    operating system provides a secure operating environment and wherein the secure mode

    involves input/output conversions. (column 5, lines 13-35)

In reference to claim 12:

England et al discloses a method comprising: (Column 7, lines 50-56) & (Column 12, line 25-

Column 13, line 50) & (Column 8, line 25-52)

- Establishing an isolated execution environment having an isolated execution mode by

    providing hardware support for the isolated execution mode, where the isolated execution

    environment is an secure execution mode, where the hardware support for the isolated

    execution mode is provided in the Access control table of (Figure 3), further described in

    (Column 6, lines 45-50) & (Column 6, line 65 – Column 7, line 5) The access control

    table is a hardware circuit, in particular a memory(Column 6, lines 33-35) whose

    information causes the gates to pass or block processor read/write controls.

- Preventing access to output data by any requester not operating in an isolated mode, where the output area where output data is written to is protected from external modification or access.

In reference to claim 13:

England et al. discloses the method of claim 12 wherein establishing comprises:

- Segregating a system memory into an isolated output area and a non-isolated area. (Figure 2) & (Column 5, lines 55 – Column 6, line 32)

In reference to claim 15:

England et al. (Column 12, lines 25 – Column 13, line 50) & (Column 7, line 50-line 56) & (Column 8, line 25-52) discloses the method of claim 13 wherein preventing comprises:

- Identifying if an isolated attribute is present in a request for access to the requested output area, where the isolated attribute is a CC code attached to requests to indicate it is part of the secure operating mode. And Denying the request if no isolated attribute is present, where the attribute is denied if no CC code is found, or it is improper.

In reference to claim 16:

England et al. (Column 12, lines 25 – Column 13, line 50) & (Column 7, line 50-line 56) & (Column 8, line 25-52) discloses the method of claim 13 further comprising:

- Loading data from the isolated output area into a bit plane on a graphics card, where the bit plane is the frame buffer.

- Denying all external access to the bit plane, where external access is denied by

  unauthorized access attempts.

In reference to claim 19:

England et al. discloses a platform comprising:

- A processor executing in one of a normal execution mode and an isolated execution

  mode; (Column 5, lines 35-55)

  - The processor including an isolated execution circuit to provide hardware support

    for the isolated execution mode where the hardware support for the isolated

    execution mode is provided in the Access control table of (Figure 3), further

    described in (Column 6, lines 45-50) & (Column 6, line 65 – Column 7, line 5)

    The access control table is a hardware circuit, in particular a memory(Column 6,

    lines 33-35) whose information causes the gates to pass or block processor

    read/write controls.

- A direct memory access controller to issue requests for access to an isolated output area;

  (Column 12, lines 25 – Column 13, line 50) & (Column 7, line 50-line 56) & (Column 8,

  line 25-52)

- A first interface coupled to the DMA controller to forward requests to a memory control

  hub (MCH); (Column 12, lines 25 – Column 13, line 50) & (Column 7, line 50-line 56) &

  (Column 8, line 25-52)

- A second interface coupled to the DMA controller to supply output data to an output

  device. (Figure 1, Item 171, 172) & (Column 4, lines 40-55)

In reference to claim 20:

England et al. discloses the apparatus of claim 19 wherein the first interface is a secure

accelerated graphics port (AGP) and the output device is a display. (Column 4, lines 15-40)

In reference to claim 21:

England et al. discloses the apparatus of claim 19 wherein the DMA controller attaches an

isolated attribute to any isolated output area access request, where the isolated attribute is a CC

code. (Column 6, lines 19-65) & (Column 7, lines 50-56)

In reference to claim 22:

England et al. discloses the apparatus of claim 19 wherein the second interface is an audio

interface. (Column 4, lines 40-55) & (Column 13, lines 20-50)

Claim Rejections - 35 USC § 103

6.   The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7.   Claims 2-5, 7-11, 14, 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over

England et al. US patent 6775779.

In reference to claim 2:

England et al. fails to explicitly disclose the platform of claim 1, wherein the output device is a

graphics card.

England et al. however teaches a method of protecting content through a method of secure

processor modes combined with secure memories. (Abstract) & Figure 2)

England et al. additionally discloses that among this content, there may be audio and video

content. It is further disclosed that access to these modules and drivers by requests external to

the secure mode are restricted. (Column 2, lines 5-15) & (Column 2, line 65 – Column 3, line

10)

England et al. further discloses that the hardware components used may include that which is

standard to a conventional PC. (Column 4, lines 15-40) and among the I/O devices that may

serve as the isolated output area includes frame buffers. (Column 13, lines 1-50)

A search of the prior art has uncovered that PC frame buffers are frequently called graphics

cards.

Framebuffer

From Wikipedia, the free encyclopedia
(Redirected from Frame buffer)

*The **framebuffer** is a video output device that drives a video display from a memory buffer containing a complete frame of data. The information in the buffer typically consists of color values for every **pixel** (point that can be displayed) on the screen. Color values are commonly stored in 1-bit **monochrome**, 4-bit **palletized**, 8-bit **palletized**, 16-bit **highcolor** and 24-bit **truecolor** formats. An additional **alpha channel** is sometimes used to retain information about pixel transparency. The total amount of the memory required to drive the framebuffer is dependent on the **resolution** of the output signal, as well as the **color depth** and **palette** size. Framebuffers differ significantly from the **vector graphics displays** that were common prior to the advent of the framebuffer. With a vector display, only the **vertices** of the graphics primitives are stored. The electron beam of the output display is then commanded to move from vertex to vertex, tracing an analog line across the area between these points. With a framebuffer, the electron beam (if the display technology uses one) is commanded to trace a left-to-right, top-to-bottom path across the entire screen, much in the same way a television renders a broadcast signal. The color information for each point on the screen is then pulled from the framebuffer, creating a set of discrete picture elements (**pixels**).*

*(**PC** framebuffers are commonly referred to as "Graphics Cards"), many users assume that a framebuffer is simply an area of memory for storing graphics.*

Although England et al. does not explicitly recite the limitation of a graphics card, in light of the disclosures of the prior art, it would have been obvious to one of ordinary skill in the art to use graphics cards as part of the isolated output area, where the output of England et al. is written to (Column 13, lines 1-5) in order to preserve the security of secure system by regulating access to output data written to the video memory.

In reference to claim 3:

England et al. discloses the platform of claim 2 further comprising:

- A memory control hub (MCH) coupled between the system memory, and the processor

  and the graphics card, the memory control hub to permit the graphics card to access the

  isolated output area only when the graphics card is asserts an isolated access mode, where

  the directed memory controller in the Access control table is the Memory control Hub

  (Column 6, lines 45 – Column 7, line 5) which directs the processor regarding the

  specific modes of execution of the executing code. This in turn controls the processor

  execution modes, and thus the output to the graphics cards where the graphics card is the

  video output adaptor with the frame buffer, and access to the frame buffer output is only

  permitted when in the secure mode. (Column 8, lines 25-53) & (Column 12, lines 25-67)

  & (Column 13, lines 1-18) & (Column 13, lines 37-50) & (Column 7, lines 50-55).

In reference to claim 4:

England et al. discloses the platform of claim 3 wherein the graphics card comprises:

- A direct memory access (DMA) controller and wherein local storage of the data from the

  isolated output area is not permitted, where attempts to transfer and store data from the

  output area to local storage such as memory is interdicted. (Column 7, lines 50-55) &

  (Column 13, lines 37-50)

In reference to claim 5:

England et al. discloses the platform of claim 3 wherein only the graphics card is permitted to read the isolated output area. (Column 12, lines 57-67) & (Column 13, lines 1-18) & (Column 10, lines 49-57)

In reference to claim 7:

England et al. discloses the platform of claim 3 further comprising:

A link between the graphics card and the MCH having an isolated transaction type, where the isolated transaction type is indicate by the secure CC number indication. (Column 12, lines 25-Column 13, line 15) & (Column 6, line 19-32)

In reference to claim 8:

England et al. discloses the platform of claim 3 wherein the MCH only permits the O/S nub to write to the isolated output area. (Column 12, line 25 – Column 13, line 50) & (Column 7, line 50-56) & (Column 8, line 25-52)

In reference to claim 9:

England et al. discloses the platform of claim 7 wherein the link is a secure accelerated graphics port bus, where the accelerated graphics port bus is an AGP port bus. (Column 4, line 15-40)

In reference to claim 10:

England et al. (column 6, lines 25-32) & (Column 12, line 25 – Column 13, line 50) discloses the platform of claim 2 wherein the graphics card comprises:

- An isolated bit plane, where the isolated bit plane is the memory of the frame buffer in secure more.

- A non-isolated bit plane, where the non isolated bit plane is the memory of the frame buffer when in unprotected mode.

In reference to claim 11:

England et al. (Column 12, line 25 – Column 13, line 50) discloses the platform of claim 10 wherein the graphics card denies all external access to the isolated bit plane.

In reference to claim 14:

England et al. discloses the method of claim 13 further comprising:

- Issuing an isolated direct memory access (DMA) request for display data in the isolated output area from a graphics card; (Column 12, lines 25 – Column 13, line 50)

- Refreshing the display based on the display data, where refreshing to display based on the display data is inherent to the function and purpose of a frame buffer. (Column 13, lines 1-15)

8.   Claims 17, 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over England et al. US patent 6775779 and Cunnif et al, US patent 6476806.

In reference to claim 17:

England et al. fails to disclose the method of claim 16 further comprising :

Defining a first window for display of an image corresponding to the bit plane; and occluding all

windows but the first window.

Cunnif et al. (Column 2, lines 25-46) discloses a bounding box that is created to enclose all the

primitives within that object. If it is determined that no pixels would be modified if the bounding

box is rendered, then the objects behind the bounding box or "window" can be considered

occluded.

Cunnif et al. discloses that occluding an object that doesn't need to be rendered would decrease

processing throughput. If computer user has open three windows, and currently one of them is

maximized, then the graphical procsessing does not have to be performed in the other windows

that are not currently displayed. It would have been obvious to one of ordinary skill in the art at

the time of invention to occlude all windows but the first window in order to decrease the

processing throughput and increase the speed of the overall processing load.

In reference to claim 18:

England et al. discloses the method of claim 13 further comprising:

- Retrieving data from the isolated output area, where the value of the secure memory may

  be accessed to a request being in secure mode. (Column 12, lines 25 – Column 13, line

  50)

- Displaying an image corresponding to the data, where displaying an image corresponding to the data is inherent to the functioning of a frame buffer.

England et al. fails to disclose :

- Occluding the image prior to a platform transitioning out of isolated execution mode.

Cunnif et al. (Column 2, lines 40-45) & (Column 5, lines 8-36) discloses a method of occluding a part of an image based on the mode of execution or a mode of the processor, and will occlude images in one mode, prior to switching to another mode.

England et al. (Column 12, lines 25 – Column 13, line 50) teaches that memory mapped IO devices such as a frame buffer should not have their information be read by untrusted software. It would have been obvious to one of ordinary skill in the art at the time of invention to occlude the image information in the frame buffer in order to prevent other non-secure software and access requests from accessing the information.

Conclusion

9.   Any inquiry concerning this communication from the examiner should be directed to Thomas M Ho whose telephone number is (571)272-3835. The examiner can normally be reached on M-F from 9:30 AM - 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor,

Gilberto Barron can be reached on **(571)272-3799**

The Examiner may also be reached through email through **Thomas.Ho6@uspto.gov**

Any inquiry of a general nature or relating to the status of this application or proceeding should

be directed to the receptionist whose telephone number is (571)272-2100.

General Information/Receptionist   Telephone: 571-272-2100   Fax: 571-273-8300
Customer Service Representative   Telephone: 571-272-2100   Fax: 571-273-8300

TMH

November 9th, 2006

GILBERTO BARRON JR
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100